UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
TYLER DIVISION

FENNER INVESTMENTS, LTD.,

Plaintiff,

v.

3COM CORPORATION,
EXTREME NETWORKS, INC.,
NETGEAR, INC.,
D-LINK SYSTEMS, INC.,
SMC NETWORKS, INC.,
TELLABS, INC.,
TELLABS NORTH AMERICA, INC., AND
ENTERASYS NETWORKS, INC.,

Defendants.

Case No.: 6:08-CV-00061 (LED)

JURY TRIAL

DEFENDANTS' REVISED RESPONSIVE CLAIM CONSTRUCTION BRIEF

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I. INTRODUCTION AND BACKGROUND

A. General

Peter Fenner, the named inventor of the patents-in-suit, United States Patent Nos. 5,842,224 and 7,145,906 ("the Fenner patents"), did not invent networks, routing, or the Internet. Instead, the invention he sought to protect in the Fenner patents is simply one solution to the problem of communicating over the Internet with mobile devices. One known alternative was to change the addresses of a device when it moves. This alternative, however, suffers from the unfortunate complexity of having to send a device's new address to all other devices on the network that may be interested in communicating with that device. Another known alternative was to assign the device a fixed and unchanging address regardless of its location, but this creates a different problem. All the network nodes that route packets, called routers or switches, must learn the actual locations of all the mobile devices to direct the packets properly. As the number of network devices increases, the tables those nodes use to match the fixed addresses with the physical locations, and the look-up times to access them, become prohibitively large.

The solution in the Fenner patents combines fixed, unique, and unchanging identification codes with arithmetic coding (compression) to make tables and address searches more manageable. As Mr. Fenner stated:

> The invention relates to a system for routing a message . . . [with e]ach end user [being] assigned a fixed and unique identification code[] that does not change as the end user moves . . . . The system utilizes arithmetic data compression techniques to compress the size or length of addresses into an index value to facilitate look up.

Ex. A [U.S. Patent No. 5,095,480 prosecution history, Information Disclosure Statement dated 6/27/90] at 1-2.

The prior art attempted to do this using a technique called "hashing," but conventional hashing methods were irreversible because there was no way to recover the original address after

compression. Mr. Fenner developed a new way of processing the fixed addresses using reversible arithmetic compression that permitted recovery of the original addresses.

Unfortunately for Mr. Fenner, the Internet never adopted his technique. In continuing patent applications, including the Fenner patents in this suit, Mr. Fenner added claims with terms absent from the original specification to try to conform his patents to the technology the Internet eventually used. Despite creative efforts, however, he could not bend his patents enough to cover that technology. The specification of his patents constrained him, as did statements he made to the United States Patent and Trademark Office ("USPTO") to obtain allowance of his patents.

This lawsuit is not Mr. Fenner's first attempt to claim dominion over network technology he did not invent. In *Fenner Investments, Ltd. v. Juniper Networks, Inc.*, No. 2:05-CV-05-LED (E.D. Tex. filed Jan. 6, 2005) ("*Fenner* I"), he tried and failed to twist a related patent to cover standards for routing data packets in mobile phone networks. This case is the same wolf in different sheep's clothing.

B. United States Patent No. 5,842,224

Plaintiff Fenner Investments, Ltd. ("Plaintiff") has asserted claims 3, 8, and 12 from United States Patent No. 5,842,224 ("'224 Patent") (Ex. B). These claims involve a communication method and system that routes data packets based on logical addresses that are independent of the sending devices' physical addresses. Exhibit C to this brief contains the undisputed and disputed terms for these claims, and both sides' proposed constructions.

C. United States Patent No. 7,145,906

Plaintiff has also asserted claims 9, 10, 19, and 20 from United States Patent No. 7,145,906 ("'906 Patent") (Ex. D). These claims involve a packet-switching node or method that filters and forwards received packets based on certain media access controller ("MAC")

addresses of those packets. Those claims also involve filtering those packets based on certain source filtering information associated with those MAC addresses. Exhibit C to this brief also contains the undisputed and disputed terms for these claims, and both sides' proposed constructions.

II. CLAIM CONSTRUCTION PRINCIPLES[1]

A. General Principles

Claim construction is an issue of law for the court. *Markman* v. *Westview Instruments, Inc.*, 52 F.3d 967, 970-71 (Fed. Cir. 1995) (*en banc*). When construing a claim term, the court must first consult the intrinsic evidence, starting with the plain meaning, then, in order, the claims, specification, and prosecution history; only under limited circumstances should the court consider extrinsic evidence. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1314-18 (Fed. Cir. 2005) (*en banc*).

To begin with, "the words of a claim are generally given their ordinary and customary meaning," which is the "meaning that the term would have to a person of ordinary skill in the art in question . . . as of the effective filing date of the patent application." *Id.* at 1312-13. Next, the court must look to the claims at issue as well as other claims. *Id.*

Then the court "must [ ] read [the claims] in view of the specification, of which they are a part." *Id.* at 1315. "[T]he specification 'is always highly relevant to the clam construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.'" *Id.* (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)). For example, "[s]tatements that describe the invention as a whole, rather than statements that

[1] Defendants ask the Court to ignore Exhibit B to Plaintiff's Opening Brief because it is pure argument and would have forced the Brief to be longer than the mandated thirty pages had it been placed properly there. Plaintiff has refused Defendants' request to remove or shorten it.

describe only preferred embodiments, are more likely to support a limiting definition of a claim term." *C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 864 (Fed. Cir. 2004).[2] In addition, when the specification describes the "invention" as opposed to particular embodiments, the court should limit the claims to that description. *See Honeywell Int'l, Inc. v. ITT Indus., Inc.*, 452 F.3d 1312, 1318-19 (Fed. Cir. 2006) (limiting "fuel injection system component" to "fuel filter," which the specification identified it as "this invention" or "the present invention"). Moreover, the specification's repeated and consistent description of a claim term also limits the scope of that term to that description. *Microsoft Corp.* v. *Multi-Tech Sys., Inc.*, 357 F.3d 1340, 1347-48 (Fed. Cir. 2004) (limiting "sending" and "receiving" to transmission over a telephone line).

Also, when the inventor disclaims or disavows the scope of the claims in the specification, "the inventor's intention, as expressed in the specification, is regarded as dispositive." *Phillips*, 415 F.3d at 1316. Similarly:

> [w]here the general summary or description of the invention describes a feature of the invention . . . and criticizes other products . . . that lack that same feature, this operates as a clear disavowal of these other products (and processes using these products).

Astrazeneca AB v. *Mutual Pharm. Co.*, 384 F.3d 1333, 1341 (Fed. Cir. 2004).

Next, the court should consider the patent's prosecution history. *Phillips*, 415 F.3d at 1317. This includes the prosecution histories of ancestor and sibling patent applications. *See Microsoft Corp.*, 357 F.3d at 1349-51 (limiting claim construction based on arguments made in prosecuting a sibling application); *Wang Labs.*, 197 F.3d at 1384 (applying a limiting claim construction based on statements made during prosecution of the parent application, in an

[2] *See also Inpro II Licensing, S.A.R.L. v. T-Mobile USA, Inc.*, 450 F.3d 1350, 1355 (Fed. Cir. 2006) (claims do not "enlarge what is patented beyond what the inventor has described as his invention."); *SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys., Inc.*, 242 F.3d 1337, 1341 (Fed. Cir. 2001); *Wang Labs., Inc. v. Am. Online, Inc.*, 197 F.3d 1377, 1383 (Fed. Cir. 1999).

information disclosure statement). The prosecution history may also reveal that the patentee has disclaimed claim scope. *Elekta Instrument S.A. v. O.U.R. Scientific Int'l Inc.*, 214 F.3d 1302, 1308 (Fed. Cir. 2000).

Finally, the court may consider extrinsic evidence, although it is "less significant than the intrinsic record in determining the legally operative meaning of claim language." *Phillips*, 415 F.3d at 1317.

B. Structures Corresponding to Means-Plus-Function Elements

For "means-plus-function" elements governed by 35 U.S.C. § 112, paragraph 6, the court must first determine the claimed function, and then identify "what structure, if any, disclosed in the specification corresponds to the claimed function." *Cardiac Pacemakers, Inc. v. St. Jude Med., Inc.*, 296 F.3d 1106, 1113 (Fed. Cir. 2002). The patentee has the duty to clearly link the corresponding structure to the function in the specification or prosecution history as the *quid pro quo* for employing § 112, paragraph 6. *See B. Braun Med. Inc. v. Abbott Labs.*, 124 F.3d 1419, 1424 (Fed. Cir. 1997).

III. DISPUTED CLAIM TERMS

A. Terms Involving Addresses

The patents-in-suit defined the addresses used in its invention very specifically, and Plaintiff used those definitions to distinguish prior art systems that the USPTO used in its initial rejections. Consequently, the construction of claim terms involving addresses share some characteristics.

1. "Logical address" means "a fixed, unique, and unchanging identifier of a connection to the Internet represented by a series of numbers that has no internal structure to suggest network connection location."

Defendants' Proposed Construction	Plaintiff's Proposed Construction
a fixed, unique, and unchanging identifier of a connection to the internet represented by a series of numbers that has no internal structure to suggest network connection location	an address assigned within a computer network; examples include IP addresses

The parties' proposed constructions differ in three respects.[3] Defendants believe a "logical address": (1) is a fixed, unique, and unchanging identifier; (2) is represented by a series of numbers; and (3) has no internal structure to suggest network connection location. The intrinsic evidence compels these requirements, so Defendants have included them.

a) The intrinsic evidence repeatedly states the need for those three requirements in Defendants' proposed construction.

Claims 3 and 5 require the "logical address" be independent of a "physical address." Ex. B at col. 34, ll. 65-67[4], 35:21-22. This is consistent with the requirement that, unlike the physical address, which changes when a device's interface changes, the logical address is a fixed, unique, and unchanging identifier. *See id.*, 10:51-67. Plaintiff's construction includes physical addresses, and so cannot be accurate.

The specification requires that logical addresses share certain characteristics.[5] One is that such addresses be "fixed, unique[,] and unchanging." *Id.* at 2:37-46. ("The present system overcomes the disadvantages of the prior art by simply assigning a fixed, unique[,] and unchanging identification code to both host A and host B.") *Id.* There is a compelling reason for

[3] Defendants accept that a logical address is assigned within a computer network, but so are all addresses.

[4] Herein notated as column:line-line or column:line-column:line.

[5] Although the specification does not use the term "logical address," it does refer to a "logical network address." *Id.* at 2:55-58, 4:45-50, 11:12-15.

this requirement. "By managing and manipulating logical network addresses within the system, mobile-end systems can keep the same network identification code (not physical address) as they move from communication network to communication network." *Id.* at 11:12-16. "The present invention overcomes the disadvantages of the prior art by considering a flat, as opposed to hierarchical, logical routing address space with unique identifiers." *Id.* at 4:37-39.

In addition, the patents define "addresses" as "identification numbers represented by a string of symbols of known length." *Id.* at 5:34-35; *see also*, *id.* at 18:30-67; FIG. 4 ("a network address is just a sequence of binary data bits of known length"). *Id.* at 17:44-45. The specification equates the invention with a string of symbols:

> In the present system, the physical address structure is removed from the design and operation of the Internet routing by treating the message addresses as a symbol string without predetermined internal structure . . . .

Id. at 11:4-8. This excerpt also equates the invention with an address having "no internal structure," the third requirement. The patent elsewhere explains, "[t]he present invention provides a . . . routing scheme totally independent of the internal logical or physical structure of the network addresses." *Id.* at 5:30-34; *see also*, *id*. at 6:6-8 ("[T]he present system provides . . . variable length addresses with no known internal structure . . . ."). Prior art systems, on the other hand, used the node's address that changed as the node moved or as its interface changed. *See id.* at 10:58-67.

Mr. Fenner cemented the need for this requirement when, to overcome the Examiner's prior art rejections, he argued to the Examiner and the USPTO Board of Appeals, that the claimed logical address is device- and location-independent. Ex. E ['224 prosecution history, Amendment dated 4/21/97] at 11-12 ("It does not matter [on] what network or device the source then currently resides.") ; Ex. F ['224 prosecution history, Appeal Br. dated 3/2/98] at 7 ("It does not matter [on] what network or device the source then currently resides or has accessed (*sic*).").

The prosecution history provides additional evidence for the third, as well as the first, requirement. Mr. Fenner, in attempting to refute the Examiner's obviousness rejections, argued that:

> [a] message in applicant's system is routed solely in accordance with unique, fixed and unchanging codes . . . . [A] receiver in Applicant's system . . . [has] its number, address or identification code (or whatever name you want to call it) remain[] the same."

Ex. G ['480 patent prosecution history, Amendment dated 11/7/90] at 24.

Hence, the intrinsic evidence supports Defendants' construction, consistent with the conclusion this Court reached when it construed "IP address" in a related Fenner patent, U.S. Patent No. 6,819,670 ("'670 Patent") (Ex. H), as "a fixed, unchanging, and unique identifier of a connection to the internet represented by a series of numbers that has no internal structure to suggest network connection location." Ex. I [*Fenner* I, Memorandum Opinion and Order (Dkt. 389)] at 17. The '670 Patent and the '224 Patent come from the same patent family and use the terms "IP address" and "logical address," respectively, to describe the same flat address. Ex. H at 4:41-48, 5:33-42, 44:15-46:45, cover page; Ex. B at 4:37-44, 5:30-39, 34:58-35:47, cover page. Indeed, Plaintiff uses IP addresses as examples of the "logical address" in its own proposed construction.

b) Plaintiff's construction does not exclude the admitted prior art, and is not supported by the intrinsic evidence.

Plaintiff's proposed construction of "logical address" as "an address assigned within a computer network," ignores the problem the Fenner patents sought to address, the problem of mobile nodes. Ex. B at 6:63-66. For example, nothing in Plaintiff's construction excludes the prior art hierarchical addressing.

Plaintiff cites no intrinsic evidence to support its overbroad construction and misstates such evidence when attacking Defendants' constructions. First, Plaintiff opposes Defendants'

construction by arguing that claim differentiation would render Claim 11 redundant. Plaintiff Fenner Investments, Ltd.'s Opening Claim Construction Brief (Dkt. 206) ("Opening Br.") at 7. Claim 11, however, refers to a "source address," and depends indirectly from independent claim 8. The term logical address appears in claim 3, which is unrelated to claim 11. Furthermore, even with Defendants' construction of logical address, claim 11 would still differ from claim 3, because claim 11 requires other limitations, such as that the unique, fixed, and unchanging code "identif[ies] the source to each network in the plurality of networks." Ex. B at 6:14-18, 32-35. Thus, adopting Defendants' construction would not render claim 11 redundant. *See Andersen Corp. v. Fiber Composites, LLC*, 474 F.3d 1361, 1370 (Fed. Cir. 2006) (rebuttable presumption of claim differentiation not applicable when claims have other differences).

Plaintiff also makes the claim-differentiation argument for claim 4, which does depend from claim 3. Opening Br. at 7.[6] Claim 4, however, also includes several limitations unrelated to "symbols," so adopting Defendants' construction would not render claim 4 redundant. *Id.*

The intrinsic evidence compels Defendants' construction. Plaintiff offers no contrary evidence to support a different construction.

2. "Source address," "source address for logically identifying the sender of the data packet," and "destination address for logically identifying a recipient of the data packet" have the same general construction as "logical address": "a fixed, unique, and unchanging identifier that has no internal structure to suggest network connection location."

Term	Defendants' Proposed Construction	Plaintiff's Proposed Construction
source address	a fixed, unique, and unchanging identifier that has no internal structure to suggest network connection location and that is assigned to the host sending the data packet	address of origin

[6] Claim 4 recites, among others, "the first logical address includes a plurality of symbols, each symbol occupying a symbol position." Ex. B at 35:8-20.

Term	Defendants' Proposed Construction	Plaintiff's Proposed Construction
source address for logically identifying the sender of the data packet	a fixed, unique, and unchanging identifier that has no internal structure to suggest network connection location and that is assigned to the host sending the data packet	a source address (as construed herein) for logically identifying the sender of the data packet
destination address for logically identifying a recipient of the data packet	a fixed, unique, and unchanging identifier that has no internal structure to suggest network connection location and that is assigned to the host receiving the data packet	the address where something is sent that logically identifies a recipient of the data packet

Defendants' proposed constructions for these terms parallel their construction for "logical address" because the "source address" and "destination address" "logically identify" a sender and recipient of a packet, respectively. Ex. B at 36:6-8, 37-39. Therefore, these addresses are "logical addresses," one for a sender and one for a recipient, and thus have (1) a fixed, unique, and unchanging identifier, and (2) no internal structure to suggest network connection location. The reasoning in Section III-A-1 explains the basis for this proposed construction. Also, claims 8 and 12 distinguish the source and destination address as "independent of the recipient's physical media address."

Plaintiff repeats many of its arguments, attacking Defendants' proposed construction of "logical address," and Defendants refer the Court to Section III-A-1 for the rebuttal. In addition, at pages 9-10 of its Opening Brief, Plaintiff cites an example of station A sending a packet to station F with a code representing A in the source node address field and a code representing F in the destination node address field. That example, however, supports Defendants' construction because those addresses are fixed, unique, and unchanging, and have no internal structure to suggest network connection location. Ex. B at 12:35-49.

Plaintiff also disputes the inclusion of "host" in the claim construction as unduly limiting (Opening Br. at 8), but the patents consistently use the term "host" to represent packet origination or destination devices. Ex. B at 2:37-46, 6:64-66, 8:7-12, 10:52-58. Therefore,

Defendants' construction is consistent with the intrinsic evidence and the Plaintiff's own use of "host" as representing packet origination or destination devices.

3. "MAC address" means "fixed, unique, and unchanging identifier assigned to a host" because, *inter alia*, Plaintiff used those requirements to distinguish its claims from prior art.

Defendants' Proposed Construction	Plaintiff's Proposed Construction
fixed, unique, and unchanging identifier assigned to a host	physical address used by the media access controller (MAC) level defined by standards such as Ethernet, token ring, or FDDI

A MAC address is simply the address of a MAC (Media Access Controller), which is simply a "multi-way switch in each node . . . which detects the physical layer node address fields of the data packets arriving from one node and uses those addresses to route (switch or bridge) the packet to another node." Ex. D at 12:35-41. Thus, a MAC address is simply the address of a node (or host), as it simply refers to a component in that node.

Claims 9, 10, 19, and 20 of the '906 Patent provide that MAC addresses are associated with communication ports, and are in the source and destination address fields of a packet. The '906 Patent, however, explains that the problem with the prior art is "addresses refer to connections and not to the [sending] device itself." Ex. D at 1:66-2:6. As explained in Sections III-A-1 and -2, the addresses consistent with the invention must be fixed, unique, and unchanging. *Id.* at 9:20-24; *see also* 2:45-47 ("The present invention . . . [allows] each host to have a fixed unique identification code instead of an address code which changes to identify itself with whatever communication network it may [be] operating [in]." Such "fixed, unique[,] and unchanging identification code" is assigned to the sending and receiving hosts. *Id.* at 2:45-47, 8:61-63; *see also* Ex. G at 23 (citations and emphasis omitted)). Therefore "MAC address" needs this limitation to distinguish the asserted claims from the prior art the specification

repudiates. Plaintiff raises the same complaints about these constructions that Defendants addressed in Section III-A-1, so Defendants will not repeat their responses here.

The Court should reject Plaintiff's construction because it equates a "physical address" with a "MAC address." That is inconsistent with the specification because the patent explains that the invention only uses fixed, unique, and unchanging identifiers routing packets, because they remain unchanged despite the movements of a host or replacement of its hardware interface. *See* Ex. D at 2:45-47, 9:20-24, 11:41-45. Thus, the claimed invention requires addresses with a fixed, unique, and unchanging identifier assigned to the host. *Id.* at 11:55-63. The "MAC address" in the claims, which is an address in the header of a packet, is a fixed, unique, and unchanging identifier, and cannot be a physical address.

Plaintiff alleges that column 14, lines 15-22 of the '906 Patent support its notion that the physical layer address is a MAC address (Opening Br. at 22), but this citation merely refers to possible address lengths. Plaintiff also cites column 6, lines 4-7 of that patent for the same purpose, but this sentence simply refers to detecting a 48-bit physical address "in" a Media Access Controller. The claim calls for a MAC address in a field of a packet.

Construing "MAC address" as a physical address, as Plaintiff proposes, contradicts the disclosure and would thus render the claims invalid as lacking written description under 35 U.S.C. § 112, first paragraph. *See TurboCare Div. of Demag Delaval Turbomachinery Corp. v. General Elec. Co.*, 264 F.3d 1111, 1119-20 (Fed. Cir. 2001) (affirming summary judgment of invalidity of a claim that recited a spring between two components where the specification taught locating the spring at an end). Therefore, a fixed, unique, and unchanging identifier assigned to a host is not a "physical address."

B. The Specification and Prosecution History Require Construing "Associated with" or "Association with" as "Referenced in a Record Identified by a Unique Value Created by Arithmetically Compressing, as Distinct from Hashing."

Term	Defendants' Proposed Construction	Plaintiff's Proposed Construction
looking up, in a directory table stored at the node, source filtering information associated with the first logical address	retrieving source filtering information (as construed herein) contained in a record identified by a unique value created by arithmetically compressing, as distinct from hashing, the first logical address	looking up, in a directory table stored at the node, source filtering information (as construed herein) associated with the first logical address (as construed herein)
each communications port having associated with it a MAC address	each communications port is referenced in a record identified by a unique value created by arithmetically compressing, as distinct from hashing, a MAC address	each communications port having associated with it a MAC address (as construed herein)
stored association with one of the three least communications ports	stored reference to the one of the at least three communications ports in a record identified by a unique value created by arithmetically compressing, as distinct from hashing, a MAC address	No construction needed
if the source address filtering information is associated with the first MAC address	if source address filtering information (as construed herein) is in a record identified by a unique value created by arithmetically compressing, as distinct from hashing, the first MAC address	if the source address filtering information (as construed herein) is associated with the first MAC address (as construed herein)
associated with a stored protection record indicating protection of that communications port from packets containing the first MAC address as a MAC source address	referenced in a stored protection record (as construed herein), identified by arithmetically compressing, as distinct from hashing, the first MAC address, indicating that the communications port is not allowed to forward packets containing the first MAC address as a MAC source address	associated with a stored protection record (as construed herein) of that communications port from packets containing the first MAC address (as construed herein) as a MAC source address (as construed herein)

1. The intrinsic evidence limits the term "associated with" to arithmetic compression and production of a unique value.

Although "associated" has a common and ordinary meaning, Plaintiff has redefined this term in the specification and prosecution history and distinguished the type of association employed by the invention over those in the prior art. The patents-in-suit describe and criticize several prior art techniques for associating addresses with other information, such as sorted tables, tree structures, and conventional hashing techniques. Ex. B at 3:23-4:26. Noting the

shortcomings of each of those techniques, the specification describes arithmetic compression or coding as a necessary aspect of the disclosed invention for associating addresses with other information. *See* Ex. D at 11:55-66 ("The novel system of the present invention . . . is made possible by employing an arithmetic code compression technique as a hashing function for the routing table access method.") In fact, the specification equates the invention with reversible arithmetic compression. *See id.* at 4:51-55 ("[T]he present invention employs a reversible arithmetic code compression technique to reduce the logical network address of up to 128 bits to a unique integer value . . . ."); *see also*, *id*. at 6:44-63 (defining the apparatus for implementing the invention to be "an application of a novel associative memory utilizing arithmetic coding to associate a key presented to the memory with a record stored in the memory."); *see also, supra* at 1 ("[t]he invention relates to a system . . . [utilizing] arithmetic data compression techniques . . . .").

Consistent with its repudiation of other association techniques in the specification, Plaintiff also relied on arithmetic coding during prosecution of the '224 Patent to distinguish the claimed invention over the conventional hashing technique:

> To provide for faster look-up of source filtering information, the logical source address is compressed, by arithmetically coding the source address, to an integer that uniquely identifies the record of data in memory containing the source filtering information.
> . . .
> Leone discloses a bridge for interconnecting local area networks. . . . [A] hash-coded form of the address . . . is . . . used as an index to determine quickly whether or not the address is already present in local memory . . . [such] formula does not "correspond" to arithmetic coding.

Ex. F at 2-5. Therefore, the intrinsic evidence compels the Defendants' constructions.

2. The Court should reject Plaintiff's construction of "associated with" because it ignores the intrinsic evidence requiring arithmetic coding.

Plaintiff's construction does not exclude prior art, conventional hashing techniques, which the patents criticize as unsuitable for the invention. Ex. D at 3:40-44, 4:32-51. Therefore, Plaintiff's construction would eviscerate the heart of the claimed invention and render the claims invalid. *TurboCare Div.*, *supra* at 12.

The specifications did discuss dynamic hashing, but they refer to it as an optional setup, insufficient on its own, employed in a particular embodiment *in combination with* the arithmetic coding required by the invention. *See* Ex. D at 4:57-61; 6:3-8. Plaintiff's Opening Brief makes much of the statement in the specification that discloses "[employing] an arithmetic code compression technique . . . as a hashing function" (Opening Brief at 13), but that statement only reinforces the distinction between conventional hashing[7] and the reversible arithmetic coding of the invention. The specification criticizes conventional hashing technique for being one-way and irreversible, because it does not allow recovery of the original address after compression. The arithmetic coding of the Fenner patents, on the other hand, is two-way and allows recovery of the original address. Ex. D at 22:36-42.

Moreover, Plaintiff disclaimed pure hashing during prosecution.[8] Ex. F at 6-7 (noting the Examiner's agreement that "arithmetic coding is a term of art that is distinguishable from other

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[7] The Fenner patents define "hashing" as follows:

> Hashing functions have traditionally been viewed as one-way, randomized mapping of the key set into the hash space. The index computed by the hashing function could not be used to reconstruct the key.

Ex. B at 4:26-33.

[8] Plaintiff also specifically disclaimed cyclic-redundancy-check (CRC) hashing when arguing around the prior art systems cited by the Examiner. Ex. F at 4-8.

forms of hashing"). Therefore, the claims must exclude it, as Defendants' construction provides. *See SciMed*, 242 F.3d at 1342-43.

Plaintiff does not deny that its construction would cover conventional (one-way) hashing, criticized and disclaimed by the specifications, and this fact alone should doom those constructions. *Id.* Plaintiff mistakenly cites the specifications to support its construction, but the portions of the specification Plaintiff cites, such as FIGS. 2-4, actually support Defendants' construction, as they all show arithmetic coding:

> Thus in FIG. 4, the destination address 126 is compressed by the arithmetic code process 138 to obtain an integer 140 which represents the address. . . . The resulting index 136 is then used to find the unique address in the compressed address directory 130. The routing switch designs 38 and 96 shown in FIGS. 2 and 3 are specific implementations of the novel arithmetic compression process employed by this invention.

Ex. D at 18:56-67.[9]

Plaintiff again mistakenly raises a claim differentiation argument. Claim 4 refers to a second logical address, a term absent in its parent claim 3. *See Andersen*, 474 F.3d at 1370.

Finally, Plaintiff objects to Defendants' proposed substitution of "retrieving" for "looking up." Opening Br. at 11-12. Defendants believe "retrieving" and "looking up" are synonymous in the context of computer memory, which is the view Plaintiff held in a prior litigation involving a parent of the '906 patent. Ex. J [*Fenner* I, Plaintiff Fenner Investments, Ltd.'s Opening Claim Construction Brief, filed January 24, 2006] at 18 ("'[L]ooking up' means retrieving, which is what the plain and ordinary meaning would suggest.").

[9] FIG. 2 shows the parallel arithmetic computation of source and destination address index values by dedicated arithmetic logic (FIG. 2, items 72 and 70), while FIG. 3 involves the serial arithmetic computation of those index values, such that the same arithmetic computation logic (FIG. 3, item 102) processes both source and destination address sequentially.

C. Terms Involving "Physical Media"

1. Defendants will accept Plaintiff's proposed construction of "physical media" as "communication layer which controls the underlying hardware technologies."[10]

To reduce the disputes between the parties, Defendants will not contest Plaintiff's construction of "physical media."

2. Defendants' modified construction of "physical media address," as "address of hardware in the physical media (as construed herein)" differs from Plaintiff's only in specifying the address.

Defendants' Proposed Construction	Plaintiff's Proposed Construction
address of hardware in the physical media (as construed herein)	address associated with the hardware of the physical media

Plaintiff's and Defendants' constructions of this term differ in Defendants' requiring that the address be "of" the hardware in the physical media, whereas Plaintiff's uses the term "associated with." "Associated with" is vague and even implicates a portion of a claim term construed in Section III.B., *supra*. Defendants respectfully submit that their construction is more specific and definite.

3. "A physical media address for identifying a physical device for routing the data packet in physical media" means "a physical media address (as construed herein) for identifying a physical device that routes the data packet in physical media (as construed herein)."

Defendants' Proposed Construction	Plaintiff's Proposed Construction
a physical media address (as construed herein) for identifying a physical device that routes the data packet in physical media (as construed herein)	a physical media address (as construed herein) for identifying a physical device for routing the data packet in physical media (as construed herein)

The only disagreement between the parties is Plaintiff's use of the term "for routing the data packet." Defendants propose that the term "for routing the data packet" describes the

[10] Both sides agree that only the occurrence of "physical media" requiring construction is its appearance as a noun in claim 8 of the '224 Patent.

"physical device" and provide a construction that not only states such, but also accurately follows the entire claim term.

D. Corresponding Structures of Claim Terms Governed by 35 U.S.C. § 112 ¶ 6

The parties agree that the following terms in the '224 Patent are means-plus-function terms, but dispute what "corresponding structure" performs the specified functions.

1. Means for receiving a data packet

Defendants' Proposed Construction	Plaintiff's Proposed Construction
FIG. 2: Source Address Shift Buffer 48, Destination Address Shift Buffer 50, and Delay Buffer FIFO 52. FIG. 3: Octet Register 104 and Octet Delay Buffer FIFO (unnumbered). FIG. 5: Key Symbol Buffer 104. *See* Ex. K (Revised).	The means for receiving a data packet is a Media Access Controllers (Figure 2 - items 34, 40, 42, 44, 46)

Defendants do not dispute that the clause "the data packet including a physical media address for identifying a physical device for routing the data packet in physical media and a source address for logically identifying a sender of the data packet independent of the sender's physical media address" (*see* Ex. C (Revised)) is a limitation on the data packet, and is not part of the function. Plaintiff and Defendants do, however, disagree sharply on the corresponding structure because Defendants find that claim 8 only refers to one component in each of Figures 2 and 3, and Plaintiff ignores that component.

Claim 8 recites "a controller for interconnecting a first data network of the plurality of data networks to at least a second data network of the plurality of data networks." In Figure 2, however, the only device that performs such interconnection is MAC switch 38. MACs 34, 40, 42, 44, and 46 act as interfaces to various Local Area Networks (LANs). *See* Ex. B at 12:8-29. MAC switch 38 corresponds to the recited controller because it interconnects the network for which MAC 34 provides an interface to the networks for which MACs 40, 42, 44, and 46

provide interfaces (*see id.* at 12:64-67). Moreover, only switch 38 performs the source-address filtering and destination address filtering that claims 8 and 12 require of the controller. *See, id.* at 11:48-59; 13:1-6. Therefore, the structure corresponding to the means-plus-function elements in the controllers of claims 8 and 12 must be in switch 38 of Fig. 2, or in the alternative switch 96 of Fig. 3.

Plaintiff's proposed construction, however, ignores both switch 38 of FIG. 2 and switch 96 of FIG. 3, and instead includes MACs 34, 40, 42, 44, and 46. Those MACs, however, are not part of the switches that interconnect networks, so they cannot correspond to the "means for receiving."

Instead, the structure in switch 38 that performs the function of "receiving a data packet, . . . including a physical media address . . . and a source address" includes source address shift buffer 48, destination address shift buffer 50, and FIFO delay buffer 52. The specification explains:

> "In switch 38, the data and clock signals on line 36 are serially coupled to a source address shift buffer 48 and then to destination address shift buffer 50. The data is then transferred from destination shift buffer 50 to delay buffer 52 which is a first-in, first-out device."

Id. at 13:10-14.

The corresponding structure must also include any structure in alternative embodiments that meets the claimed function. The "[d]isclosed structure includes that which is described in a patent specification, including alternative structure identified." *Serrano v. Telular Corp.*, 111 F.3d 1578, 1583 (Fed. Cir. 2000). In switch 96, the corresponding devices are octet register 104 and octet FIFO delay buffer (unnumbered). *Id.* at 15:5-8. Further, for the associative memory module 500 of Figure 5, which introduces generic terminology for the associative memories of

Figures 2-4, the key symbol buffer 104 is a corresponding device that receives the data packet. *Id.* at 22:10-12, 42-49.

Because Plaintiff's proposed construction improperly excludes the MACs 38 and 96, this Court should adopt Defendants' proposed structure for "means for receiving a data packet."

2. Means for looking up in a directory table stored at the controller using the source address source filtering information associated with the source address

Defendants' Proposed Structure	Plaintiff's Proposed Structure
FIG 2: Source Address Index Table 68; Source Protect Table 78; Combine Table Output 72; Source Index Table 74; Zero Detect 90; Learned Address Logic 88 (as further described in FIG. 6 and including variations of the add key logic circuitry presented in FIGS. 7 and FIGS. 9–14, and including the symbol use count logic circuit as described in FIG. 8). FIG. 3: Source and Destination Index Tables 98; Address Record Memory 100; Arithmetic Computation 102; and Index Buffer 108. FIG 4: Arithmetic Code Compression 138; and Compressed Address Directory 130. FIG. 5: Key Index Table Memory 68'; Arithmetic Computation Logic Circuit 72'; Record Memory 78'; Record Index (Address) 74'; Learned Key Logic 88'; or, in the alternative, programmable devices implementing the logical functions of the dedicated circuitry of FIG. 5 as described above; or, in the alternative, the host system of FIG. 5 performing some or all of the processing performed by the dedicated circuitry of FIG. 5 as described above. *See* Ex. L (Revised).	The means for looking up in a directory table are the source index and the source protect table (Figure 2 - items 74 and 78). The claim language itself describes how source filtering information (as construed herein) is used for looking up in a directory table.

a) Defendants' construction accounts for all the functions and all the alternative embodiments[11]

The parties agree that the claimed function corresponding to this term is "looking up in a directory table stored at the controller using the source address source filtering information

[11] Defendants have added "Index Buffer 108" and "Record Index (Address) 74'," and have withdrawn components "Source Protect Record 80," "Learned Route Logic 94," "Source Protect Record 110," "Multicast Record List 134," "Integer 140," "Truncate 142," Mod (N) 144," and "Index 136" from the structures necessary to perform the "looking up . . ." function in claim 8. Ex. B.

associated with the source address." Opening Br. at 17. The structure necessary to perform the stated function must therefore perform the following functions: (1) looking up in a directory table (2) stored at the controller (3) using the source address (4) source filtering information associated with the source address. A substantial portion of the specification and significant portions of the structure in FIGS. 2, 3, 4, and 5 describe the structure necessary to perform "looking up" in a directory table.

The abstract initially describes the look-up function as "to generate from a key an address in memory storing an associated record." The look-up tables are "stored in a memory" and "constructed with the aid of arithmetic data compression methods."

Figure 2 discloses specific structure for looking up source address filtering information in a directory table. A Media Access Controller switch (38) processes source and destination addresses through a look-up table. Ex. B at 13:18-19, 14:56-65. The source address-handling portion of the controller (38) processes the source address data through the source index table (68), arithmetically combines the outputs of the source index table (68) in combiner (72), receives an address by the source index (74), which it uses as the address in the source protect table (78). *Id.* at 14:6-9, 13:47-52, 13:52-59, 14:45-51. The output of source protect table (78) goes to the source protection record (80) to route the data to the destination controller. *Id.* at 14:32-35. Learned address logic (88) shifts the destination and source addresses when the controller (38) handles the source address of a mobile node. *Id.* at 14:2-16.

FIG. 3 discloses an alternate controller structure (96) for processing source and destination address information. *Id.* at 14:66-15:42.

b) Plaintiff's construction ignores many features of the corresponding function, and the structure needed for those features.

Plaintiff's proposed structure includes only the source index 74 and source protect table 78,[12] which focuses only on the function of "looking up in a directory table" without the remaining functionality of this term. "It is improper to narrow the scope of the function beyond the claim language." *Cardiac Pacemakers*, 296 F.3d at 1113 (Fed. Cir. 2002).

Plaintiff's structure does not perform the function of looking up address source-filtering information using a source address, such as the source index table that processes the source address information. The source index 74 is not the "source address" but rather the stored output of the arithmetic combination of the source address. Ex. B at 13:44-55. Thus, Plaintiff improperly excludes the structure that "uses" the source address filtering information for calculating the source index. The '224 Patent, however, links the use of the source address to "look up" the source filtering information. *See* Ex. B at 13:1-5 ("FIG. 2 examines the source node address field of the incoming information to determine if any or all of the other connected nodes are protected from receiving information . . . [t]his operation is often called "source address filtering.").

Under the embodiment of FIG. 2, first "the source address fields . . . [are] shifted into buffer 48." *Id.* at 13:44-46. The source address fields are then stored in the source index table 68. *Id*. at 13:49-50. "The output of the [source index tables 68] is then arithmetically combined in combiner []70." *Id*. at 13:50-52. The arithmetic combiners further include blocks 138 (arithmetic code compression) and 130 (compressed address directory) from FIG. 4

[12] Plaintiff's Opening Brief proposes a structure different from its construction in the Joint Claim Construction and Prehearing Statement Pursuant to Patent Local Rule 4-3 which included additionally at least the "protect record 80." *See* Opening Brief at 19.

that are additionally necessary structure to complete the arithmetic combination involved in performing the "looking up" function. *See id.* at 17:40-42. ("The novel system uses arithmetic coding of the directory index 130 as shown . . . in FIG 4.").

The arithmetically combined output from combiner 72 yields the source index 74. "[S]ource index 74 is used as the address into the source protect table 78 and the output of that location is the source protection record 80." *Id*. at 13:56-58. Moreover, the source index table 68—used to perform the "looking up" function as described above—is created in part by the learned address logic 88 and the zero detect logic 90 which, accordingly, form part of the structure necessary for "looking up."[13] *Id.* at 14:2-9.

Additionally, Plaintiff's structure omits critical components necessary for the arithmetic compression at the heart of its claims. The claims require arithmetic coding applied to source and destination addresses to perform "look up" filtering or routing information. *Id.* at 4:45-49 ("[T]he present invention employs a reversible arithmetic code compression technique to reduce the logical network address of up to 128 bits to a unique integer value . . . ."); *id*. at 4:62-65 ("Arithmetic coding, when applied to addresses as known length keys, provides several advantages for table look-up . . . ."); *id*. at 6:41-43 ("This apparatus is an application of a novel associative memory utilizing arithmetic coding . . . ."); *id*. at 18:7-9 ("The routing switch designs . . . shown in FIGS. 2 and 3 are specific implementations of the novel arithmetic compression process employed by this invention."). Accordingly, the structure corresponding to "looking up

[13] The '224 Patent also describes the detailed structure necessary for the learned address logic 88 in FIG. 6. *Id.* at 7:24-25 ("FIG. 6 is schematic representation of a circuit for learned key logic."). Additional structural variations of the "add key logic" component of the "learned key logic" appear in FIGS. 7, and 9-14.

. . . using the source address" must include the structure necessary for providing the arithmetic combinations, which Defendants' proposed construction includes.

c) Plaintiff's construction ignores the alternate embodiments.

Plaintiff also improperly ignores the intrinsic evidence by failing to include structure for arithmetic coding and the alternative structures in FIGS. 3 and 5 that Defendants' proposed construction includes. Plaintiff mistakenly relies on *NOMOS Corp. v Brainlab USA*, 357 F.3d 1364 (Fed. Cir. 2004), to exclude the structure of FIGS. 3, 4, and 5. *NOMOS* does not teach limiting the corresponding structure to a single embodiment when the patent discloses several embodiments. *Id.* at 1368. In *NOMOS*, the patent only disclosed a single embodiment and thus, the corresponding structure was limited to that embodiment. *Id*.

The rule that governs this case is that the "[d]isclosed structure includes that which is described in a patent specification, including alternative structures identified." *Serrano*, 111 F.3d at 1583. FIG. 3 describes a look up manipulating the source address in serial manner as an alternative to the parallel looking up performed by FIG. 2. FIG. 5 describes a look up manipulating the source address in serial manner. Ex. B at 7:6-13, 18:7-9, 22:5-10. FIG. 5 provides an alternative embodiment with learned key logic 88 and stored record logic 94, both of which assist in accessing or looking up source addresses. *See id.* at 22:5-17, 22:31-32, 39-41. Finally "FIG. 4 . . . further illustrates the manner in which a destination address or source address can be compressed to provide a usable index for accessing the address directory." *Id.* at 7:14-23. Therefore, FIG. 4 includes structure necessary to perform the "looking up" function. Accordingly, Defendants respectfully request the Court to adopt its proposed structure for "means for looking up in a directory table stored at the controller using the source address source filtering information associated with the source address."

3. Means for looking up, using the destination address, in a routing table information associated with the destination address for routing the data packet for delivery to the receiver

Defendants' Proposed Structure	Plaintiff's Proposed Structure
FIG. 2: Learned Address logic 88 (as further described in FIG. 6 and including variations of the add key logic circuitry presented in FIGS. 7 and FIGS. 9–14, and including the symbol use count logic circuit as described in FIG. 8); Destination Index Table 66; Combine Table Output 70; Route Index 76; Destination routing table 84; and Zero Detect (unnumbered). FIG 3: Source and Destination Index Tables 98; Arithmetic Computation 102; Address Record Memory 100; and Index Buffer 108. FIG 4: Outbound Record Linked List 132; Arithmetic Code Compression 138; Compressed Address Directory 130. FIG 5: Index Table Memory 68'; Arithmetic Computation Logic 72'; Record Index (Address) 74'; Record Memory 78'; Learned Key Logic 88'; and Zero Detect 90; or, in the alternative, programmable devices implementing the logical functions of the dedicated circuitry of FIG. 5 as described above; or, in the alternative, the host system of FIG. 5 performing some or all of the processing performed by the dedicated circuitry of FIG. 5 as described above. *See* Ex. M (Revised).	The means for looking up is the routing index 76 and destination routing table 84 as shown in Figure 2 and described therein. The routing table index uses the destination address to look up information associated with the destination address.

The parties agree that the claimed function corresponding to this term of claim 12 of the '224 Patent is "looking up, using the destination address, in a routing table information associated with the destination address for routing the data packet for delivery to the receiver."[14] Ex. B at 36:41-43. The structure necessary to perform the stated function must perform all of the necessary functions of (1) looking up using the destination address (2) in a routing table (3) information associated with the destination address (4) for routing the data packet for delivery to the receiver. The first set of corresponding structures appears in FIG. 2. The switch node 38 determines if learned address logic 88 and zero detect have received the destination

[14] Defendants have added "Outbound Record Linked List 132," "Index Buffer 108," "Record Index (Address) 74'," and "Zero Detect 90," and withdrawn components "Route Record 86," "Learned Route Logic 94," "Source Protect Record 110," "Destination Route Record 112," "Line 114," "Multicast Record List 134," "Integer 140," "Truncate 142," Mod (N) 144," and "Index 136" from the structures necessary to perform the "looking up . . ." function in claim 12.

address. *See* Ex. B at 14:2-9. If the destination address has not previously been stored in the source index 68, it is stored in both the source and destination index tables 66 and 68. *Id.* "The output of [the destination index table 66] . . . is then arithmetically combined in combiner[] 70." *Id.* at 13:50-52. The arithmetic combiners further includes blocks 138 (arithmetic code compression) and 130 (compressed address directory) from FIG. 4 that are necessary structure to complete the arithmetic combination involved in performing the "looking up" function. *See id.* at 17:40-42. ("The novel system uses the arithmetic coding of the directory index 130 as shown . . . in FIG 4."). The combiner adds the destination table 66 to compute the route index 76. *Id.* at 13:55-56. "[T]he route index 76 is used as the address of a location in the destination routing table 84 and the contents of that location is [*sic*] coupled to a route record 86." *Id*. at 13:59-64. The destination routing table is "also called Outbound Record Linked List 132 in FIG. 4." *Id*. at 14:36-40.

Moreover, the corresponding structure for the "looking up, using the destination address" function must include the structures that perform arithmetic compression. *See, e.g.*, *id.* at 4:45-49 ("[T]he present invention employs a reversible arithmetic code compression technique to reduce the logical network address of up to 128 bits to a unique integer value").

As it does for its proposed structure for "means for looking up in a directory table," Plaintiff omits critical structure necessary for looking up information associated with the destination address, seeking to limit the corresponding structure only to route index 76 and destination routing table 84.[15] Plaintiff's proposed corresponding structure is improper for the reasons discussed above in Section III-F-2.

[15] Plaintiff has modified its proposed structure submitted to the court, which identified the corresponding structure as the index 136 and compressed address directory of FIG. 4.

First, Plaintiff's construction ignores that the claimed function requires "looking up, *using the destination address*." Performing the look up function requires structure that uses the "destination address" to "look up" "in a routing table information associated with the destination address for routing the data packet for delivery to the receiver."

Second, Plaintiff omits the alternative structures disclosed. The corresponding structure for "looking up, using the destination address . . ." must include the alternative structures for the claimed function disclosed in the specification. *Serrano*, 111 F.3d at 1583. As explained above in Sections III-F-1 and 2, the '224 Patent includes alternative structures in FIGS. 2, 3, and 5.

4. Means for filtering the data packet in response to the source filtering information

Defendants' Proposed Structure	Plaintiff's Proposed Structure
FIG. 2: Protect Record 80, and Buffered Routing Logic 56. FIG 3: Source Protect Record 110; Buffered Routing Logic (unnumbered). FIG 4: Multicast Record List 134. FIG 5: Output Lines 519, Record Buffer 80'; and Delay Element 515 or, in the alternative, programmable devices implementing the logical functions of the dedicated circuitry of FIG. 5 as described above, or, in the alternative, the host system of FIG. 5 performing some or all of the processing performed by the dedicated circuitry of FIG. 5 as described above. *See* Ex. N (Revised).	The means for filtering the data packet is the buffered routing logic (Figure 2 – item 56). The data is filtered in response to the source filtering information (as construed herein).

The parties agree that the claimed function for this term is "filtering the data packet in response to the source filtering information."[16] Plaintiff's proposed corresponding structure,

[16] Defendants withdraw components "learned route logic 94," "Source and Destination index tables 98," "Arithmetic computation 102," "Address Record Memory 100," "Destination Route Record 112," "Line 114," "Index Table Memory 68," "Arithmetic Computation Logic 72," "Record Memory 78'," and "Learned Address Logic 88" from the structures necessary to perform the "means for filtering . . ." function in claim 8. Those components are related to the "look up" function rather than the "filtering" function. Defendants' proposed corresponding structures in FIG. 5 adds structure "output lines 519, and "delay element 515" which were not included in Defendants' construction set forth in the Joint Claim Construction Statement.

however, improperly omits structure necessary to perform the filtering function and excludes the alternative structures for this function in the '224 Patent. *See Serrano*, 111 F.3d at 1583.

The structure necessary to "filter the data packet in response to the source filtering information" includes the protect record 80[17] and the buffered routing logic 56 in FIG. 2. *See* Ex. B at 13:61-65 ("The outputs of the protect record 80 . . . are used by the routing logic 56 . . . to determine which destination MAC is to receive the message."). Moreover, the alternative structures in FIG. 3 include the source protect record 110 and the buffered routing logic 56.

Finally, FIG. 5 discloses yet another structure that "filter[s] the data packet," which includes record memory 78, output lines 519, record buffer 80, delay element 515, and buffered routing logic. *See id.* at 24:13-22.

IV. CONCLUSION

For the reasons above, Defendants respectfully ask the Court to adopt their proposed constructions because they are consistent with the intrinsic evidence and follow the Federal Circuit's instructions on construing claims. Plaintiff's proposed constructions, in contrast, ignore the intrinsic evidence and the applicable law.

[17] The source protect record 80 is also called the Multicast Record List in FIG. 4. Ex. B at 14:25-27.

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Respectfully submitted,

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The undersigned hereby certifies that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3) on this 14th day of April, 2009. All other counsel not deemed to have consented to service in such manner will be served via facsimile transmission and/or first class mail.

/s/ Trey Yarbrough
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